As a below named inventor, I declare: that I verily believe myself to be the original, first and sole (if only one individual inventor is listed below) or an original, first and joint inventor (if more than one individual inventor is listed below) of the invention in

SEMICONDUCTOR INTEGRATED CIRCUIT HAVING LATCHING MEANS CAPABLE OF SCANNING

the	specification	o f	which	is	attached	hereto	unless	the	following	box	i s
chec	ked.										

was filed on	as	Unite	ed States	App	lication
or PCT International Application	n l	No			and
was amended on		(if ar	plicable)		

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information of which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365 (b) of any foreign application(s) for patent or inventor's certificate, or 35 U.S.C. 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also

Country Category Application No. Filing Date Priority

Japan Patent 2001-304750 September 28, 2001 Yes

identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the

application on which priority is claimed:

I hereby appoint the registrants of Oblon, Spivak, McClelland, Maier & Neustadt, P.C., Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202, Customer No. 22850, or any one of them. Send correspondence to Oblon, Spivak, McClelland, Mailer & Neustadt, P. C., Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202, Telephone No. (703) 413-3000.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

DECLARATION FOR PATENT APPLICATION

I declare further that my mailing address is at c/o Intellectual Property Division, KABUSHIKI KAISHA TOSHIBA, 1-1 Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan; and that my citizenship and residence are as stated below next to my name:

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